REMARKS

Status of Claims

Claims 1 - 5 have been cancelled.

Claims 6 – 10 are new claims by this amendments.

Claim Rejections – 35 USC §102

Claims 1-5 have been rejected under 35 USC § 102 (a and e) as being anticipated by Berenbaum et al.

Claims 1 – 5 have been cancelled.

The Applicant, in view of the amendments, respectfully traverses the rejections with the following arguments.

[Argument 1]: The current invention claims "the at least one global register file is partitioned into at least one sub-register file" (supported by Fig. 1 of the current invention). The cited prior art, Berenbaum et al, failed to teach the claimed limitation. Examiner is respectfully requested to provide a prima facie evidence for such a rejection.

[Argument 2]: The current invention claims "the at least one sub-register file can map to at least two clustered functional units respectively" (supported by Fig. 1 of the current invention). The cited prior art, Berenbaum et al, failed to teach the claimed limitation. Examiner is respectfully requested to provide a prima facie evidence for such a rejection.

[Argument 3]: The current invention claims "each of the at least one local register file maps to one of the clustered function units, wherein establishing a mapping relationship between a global register file, a local register file, and a clustered functional unit" (supported by Fig. 1 of the current invention). The cited prior art, Berenbaum et al, failed to teach the claimed limitation. Examiner is respectfully requested to provide a prima facie evidence for such a rejection.

[Argument 4]: The current invention claims "the clustered functional units exchange data, … without transferring the data". The cited prior art, Berenbaum et al, failed to teach the claimed limitation. Examiner is respectfully requested to provide a prima facie evidence for such a rejection.

[Argument 5]: The current invention claims "the clustered functional units exchange data by permutation of the sub-register files of the at least one global register file through setting crossbar switches". The cited prior art, Berenbaum et al, failed to teach the claimed limitation. Examiner is respectfully requested to provide a prima facie evidence for such a rejection.

[Argument 6]: The current invention claims "the permutation maps the sub-register files of the at least one global register file to the clustered functional units." The cited prior art, Berenbaum et al, failed to teach the claimed limitation. Examiner is respectfully requested to provide a prima facie evidence for such a rejection.

[Argument 7]: Berenbaum et al teach "instruction packet splitting" that a VLIW processor selectively issues and process a portion of the bundled VLIW instruction within a cycle. The non-selected portions of the bundled VLIW instruction are issued and processed by subsequent cycles. The current invention disclosed "permutation of sub-register files of a global register file" for each functional unit to access the desired exchanging data directly to a storage (global register file) where the functional unit was not formerly associated with. The datum remains at where it is stored. The route of data accesses of each function unit is changed through the permutation.

In view of the amendments and remarks, Applicant submits that all of the pending claims are in condition for allowance and requests early and favorable action on the merits. The Examiner is invited to telephone the undersigned, Applicant's Attorney of Record, to facilitate advancement of the present application.

Respectfully submitted,

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Date

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